WHAT IS CLAIMED IS:

1. A semiconductor device including an element active region defined by forming an element isolation structure on a semiconductor substrate, comprising:

an island-like charge storage film formed across said element isolation structure and said element active region so as to be formed on said element active region through an insulating film,

said charge storage film having a recess in a surface on said element active region and a hole formed on said element isolation structure to reach said element isolation structure;

a dielectric film so formed as to cover the surface of said charge storage film including inner surfaces of said hole; and

a conductive film formed on said dielectric film.

2. A device according to claim 1, wherein said charge storage film and said conductive film function as a floating gate and a control gate, respectively, thereby constituting a semiconductor memory.

3. A device according to claim 1, wherein said charge storage film is formed on each of a plurality of element isolation regions, and adjacent charge storage films are separated from each other with a spacing not less than twice a width of said recess.

4. A device according to claim 1, wherein said element isolation structure is selected from the group consisting of a field oxide film formed by LOCOS, a trench type element isolation structure, and a field shield element isolation structure.

5. A device according to claim 1, wherein said dielectric film contains a material selected from the group consisting of a ferroelectric film and a high dielectric film, and

at least one of said charge storage film and said conductive film contains a material selected from the group consisting of a titanium compound, a tungsten compound, a ruthenium compound, and platinum.

6. A device according to claim 2, wherein said semiconductor memory is a multivalue nonvolatile memory which can store one among different store states represented by three values or more.

7. A device according to claim 1, wherein said charge storage film comprises a film selected from the group consisting of an insulating film including a silicon nitride film, an insulating film including a silicon oxide film and a silicon nitride film, and a conductive film.

8. A semiconductor device including an element active region defined by forming an element isolation structure on a semiconductor substrate, comprising:

an island-like charge storage film formed across said element isolation structure and said element active region so as to be formed on said element active region through an insulating film,

said charge storage film having a recess in a surface on said element active region and a hole formed on said element isolation structure to reach said element isolation structure; and

a conductive film formed on said charge storage film.

9. A device according to claim 8, wherein said charge

storage film comprises a film selected from the group consisting of an insulating film including a silicon nitride film, an insulating film including a silicon oxide film and a silicon nitride film, and a conductive film.

10. A semiconductor device including an element active region defined by forming an element isolation structure on a semiconductor substrate and having a transistor constituted by a gate electrode and a pair of impurity diffusion layers in said element active region, comprising:

an insulating interlayer formed on said semiconductor substrate including said transistor;

a first hole formed in said insulating interlayer and having a surface layer of said impurity diffusion layer as a bottom surface;

an island-like charge storage film electrically connected to one of said impurity diffusion layers through said first hole;

a second hole formed in said charge storage film and having a surface layer of said insulating interlayer as a bottom surface;

a dielectric film so formed as to cover a surface of said charge storage film including inner surfaces of said second hole; and

a conductive film formed on said dielectric film ,

wherein said charge storage film, said dielectric film, and said conductive film constitute a capacitor.

11. A device according to claim 10, wherein said dielectric film contains a material selected from the group consisting of a ferroelectric film and a high dielectric film, and

at least one of said charge storage film and said conductive film contains a material selected from the group consisting of a titanium compound, a tungsten compound, a ruthenium compound, and platinum.

12. A device according to claim 10, wherein said semiconductor device is a multivalue DRAM which can store one among different store states represented by three values or more.

13. A device according to claim 10, wherein said charge storage film comprises a film selected from the group consisting of an insulating film including a silicon nitride film, an insulating film including a silicon oxide film and a silicon nitride film, and a conductive film.

14. A semiconductor device including an element active region defined by forming an element isolation structure on a semiconductor substrate, comprising:

an insulating film formed on said semiconductor substrate in said element active region; and

a charge storage film patterned on said insulating film,

wherein said charge storage film is formed across said element isolation structure and has a hole on said element isolation structure, and

at least a portion of a bottom surface of said hole reaches a surface layer of said element isolation structure.

15. A device according to claim 14, wherein said element isolation structure is selected from the group consisting of an element isolation structure made from an insulating film and an element isolation structure

including an electrode for isolation.

16. A device according to claim 14, further comprising:

a dielectric film formed on said charge storage film including inner surfaces of said hole; and

a conductive film formed on said dielectric film.

17. A device according to claim 14, wherein said charge storage film functions as a floating gate of a nonvolatile transistor.

18. A device according to claim 16, wherein said dielectric film contains a material selected from the group consisting of a ferroelectric film and a high dielectric film, and

at least one of said charge storage film and said conductive film contains a material selected from the group consisting of a titanium compound, a tungsten compound, a ruthenium compound, and platinum.

19. A device according to claim 14, wherein said semiconductor device is a multivalue memory which can store one among different store states represented by three values or more.

20. A device according to claim 14, wherein said charge storage film comprises a film selected from the group consisting of an insulating film including a silicon nitride film, an insulating film including a silicon oxide film and a silicon nitride film, and a conductive film.

21. A semiconductor device including a plurality of element isolation regions defined by forming an element isolation structure on a semiconductor substrate, comprising:

an island-like charge storage film formed across said

element isolation structure and said element active regions and having a recess;

a dielectric film so formed as to cover a surface of said charge storage film; and

a conductive film formed on said dielectric film and capacitively coupled with said charge storage film,

wherein said charge storage film is formed in each of said element active regions, and an upper surface of each of said charge storage films is planarized by CMP and flush with an upper surface of an adjacent charge storage film.

22. A device according to claim 21, wherein said element isolation structure is selected from the group consisting of a field oxide film formed by LOCOS, a trench type element isolation structure, and a field shield element isolation structure.

23. A device according to claim 21, wherein a hole reaching said element isolation structure is formed in a portion of said charge storage film above said element isolation structure.

24. A device according to claim 21, wherein a bottom surface of said recess is substantially flush with or lower than a surface of said element isolation structure.

25. A device according to claim 21, wherein said dielectric film contains a material selected from the group consisting of a ferroelectric film and a high dielectric film, and

at least one of said charge storage film and said conductive film contains a material selected from the group consisting of a titanium compound, a tungsten compound, a ruthenium compound, and platinum.

26. A device according to claim 21, wherein said charge storage film and said conductive film function as a floating gate and a control gate, respectively, thereby constituting a semiconductor memory.

27. A device according to claim 21, wherein said charge storage film comprises a film selected from the group consisting of an insulating film including a silicon nitride film, an insulating film including a silicon oxide film and a silicon nitride film, and a conductive film.

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28. A method of fabricating a semiconductor device, comprising:

the first step of defining an element active region by forming an element isolation structure on a semiconductor substrate;

the second step of forming an insulating film on said semiconductor substrate in said element active region;

the third step of forming a first conductive film on an entire surface of said semiconductor substrate including said insulating film and said element isolation structure;

the fourth step of forming a mask pattern having first and second openings on said first conductive film;

the fifth step of etching said first conductive film until said element isolation structure is exposed in said first opening by using said mask pattern as a mask, thereby dividing said first conductive film, and simultaneously forming a recess in said second opening by leaving said first conductive film behind on a bottom;

the sixth step of forming a dielectric film so as to cover a surface of said first conductive film; and

the seventh step of forming a second conductive film on

said dielectric film and opposing said second conductive film to said first conductive film through said dielectric film.

29. A method according to claim 28, further comprising, after the seventh step, the eighth step of doping an impurity into said semiconductor substrate in said element active region to form a pair of impurity diffusion layers in surface regions of said semiconductor substrate on two sides of said first conductive film.

30. A method according to claim 28, wherein in the fourth step, said mask pattern is so formed that a width of said first opening is not less than twice a width of said second opening.

31. A method according to claim 28, further comprising, between the third and fourth steps, the ninth step of planarizing said first conductive film by polishing, and

wherein in the fourth step, said mask pattern is so formed that said second opening is positioned above said element active region.

32. A method of fabricating a semiconductor device, comprising:

the first step of defining an element active region by forming an element isolation structure on a semiconductor substrate;

the second step of forming a gate insulating film and a gate electrode in said element active region;

the third step of doping an impurity into said second substrate to form a pair of impurity diffusion layers in surface regions of said semiconductor substrate on two sides of said gate electrode;

the fourth step of forming a first conductive film electrically connected to one of said impurity diffusion layers;

the fifth step of forming a mask pattern having at least first and second openings on said first conductive film;

the sixth step of etching said first conductive film by using said mask pattern as a mask, thereby dividing said first conductive film in said first opening, and simultaneously forming a recess in said second opening by leaving said first conductive film behind on a bottom;

the seventh step of forming a dielectric film so as to cover a surface of said first conductive film; and

the eighth step of forming a second conductive film on said dielectric film and opposing said second conductive film to said first conductive film through said dielectric film.

33. A method according to claim 32, further comprising, between the third and fourth steps,

the ninth step of forming an insulating interlayer on an entire surface of said semiconductor substrate, and

the 10th step of forming a hole in said insulating interlayer in which one of said impurity diffusion layers is exposed, and

wherein in the fourth step, a first conductive film is formed on said insulating interlayer and said hole is filled with said first conductive film, and

in the sixth step, said first conductive film is etched until said insulating interlayer is exposed in said first opening.

34. A method according to claim 32, wherein in the seventh step, said mask pattern is so formed that a width of said first opening is not less than twice a width of said second opening.

35. A method according to claim 32, further comprising, between the fourth and fifth steps, the 11th step of planarizing said first conductive film by polishing, and

wherein in the fifth step, said mask pattern is so formed that said second opening is positioned above said element active region.

36. A method of fabricating a semiconductor device, comprising:

the first step of forming a first conductive film in an insulating film region on a semiconductor substrate;

the second step of forming a mask pattern having two types of openings on said first conductive film;

the third step of etching said first conductive film by using said mask pattern as a mask, thereby dividing said first conductive film conforming to a shape of one of said openings and simultaneously forming at least one recess in a surface of said divided first conductive film conforming to a shape of the other opening;

the fourth step of forming an insulating film so as to cover a surface of said first conductive film; and

the fifth step of forming a second conductive film so as to cover a surface of said insulating film and opposing said second conductive film to said first conductive film through said insulating film.

37. A method according to claim 36, wherein in the third step, said recess is so formed as to reach said

insulating film region, thereby forming a hole in which a surface of said insulating film region is exposed.

38. A method of fabricating a semiconductor device, comprising:

the first step of defining an element active region by forming an element isolation structure on a semiconductor substrate;

the second step of forming an insulating film on said semiconductor substrate in said element active region;

the third step of forming a first conductive film on an entire surface including said insulating film and said element isolation structure;

the fourth step of forming a mask pattern having at least first and second openings on said first conductive film;

the fifth step of etching said first conductive film until said element isolation structure is exposed in said first and second openings by using said mask pattern as a mask, thereby dividing said first conductive film below said first opening and simultaneously forming a hole extending through said first conductive film below said second opening;

the sixth step of forming a dielectric film so as to cover said first conductive film; and

the seventh step of forming a second conductive film on said dielectric film and opposing said second conductive film to said first conductive film through said dielectric film.

39. A method according to claim 38, further comprising, after the seventh step, the eight step of doping an

impurity into said semiconductor substrate in said element active region to form a pair of impurity diffusion layers in surface regions of said semiconductor substrate on two sides of said first conductive film.

40. A method according to claim 38, further comprising, between the third and fourth steps, the ninth step of planarizing said first conductive film by polishing.

41. A method according to claim 38, wherein in the first step, a field shield element isolation structure in which a shield plate electrode is embedded is formed on said semiconductor substrate.

42. A method of fabricating a semiconductor substrate, comprising:

the first step of defining an element active region by forming an element isolation structure on a semiconductor substrate;

the second step of forming a gate oxide film and a gate electrode on said semiconductor substrate in said element active region;

the third step of doping an impurity into said semiconductor substrate in said element active region to form a pair of impurity diffusion layers in surface regions of said semiconductor substrate on two sides of said gate electrode;

the fourth step of forming a first conductive film electrically connected to one of said impurity diffusion layers;

the fifth step of forming a mask pattern having at least first and second openings on said first conductive film;

the sixth step of etching said first conductive film by using said mask pattern as a mask, thereby dividing said first conductive film below said first opening, and simultaneously forming a hole extending through said first conductive film below said second opening;

the seventh step of forming a dielectric film so as to cover a surface of said first conductive film; and

the eighth step of forming a second conductive film so as to cover said dielectric film and opposing said second conductive film to said first conductive film through said dielectric film.

43. A method according to claim 42, further comprising, between the third and fourth steps,

the ninth step of forming an insulating interlayer on an entire surface of said semiconductor substrate, and

the 10th step of forming a hole in said insulating interlayer in which one of said impurity diffusion layers is exposed, and

wherein in the fourth step, a first conductive film is formed on said insulating interlayer and said hole is filled with said first conductive film, and

in the sixth step, said first conductive film is etched until said insulating interlayer is exposed in said first and second openings.

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44. A method according to claim 42, further comprising, between the fourth and fifth steps, the ninth step of planarizing said first conductive film by polishing.

45. A method according to claim 42, wherein in the first step, a field shield element isolation structure in which a shield plate electrode is embedded is formed on said

semiconductor substrate.

46. A device according to claim 1, wherein a source and a drain regions are formed in said element active region on both sides of said electric charge accumulation film,and

said source region is formed commonly to adjacent element active regions.

47. A device according to claim 1, further comprising an access transistor adjacently formed to said electric charge accumulation film.